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PTO/SB/122 (11-96)

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Application Number	09/652,550
Filing Date	August 31, 2000
First Named Inventor	Keiji Jono
Group Art Unit	2811
Examiner Name	T. F. Tran
Attorney Docket Number	KMI-001

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Practitioner's Docket No. KM1-001

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jono et al., Keiji

Application No.: 09/652,550

Group No.: 2811

Filed: 08/31/00

Examiner: T.F. Tran

For: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

Assistant Commissioner for Patents  
Washington, D.C. 20231

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